



SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

MOSCONE WEST CENTER
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Advancing power signoff for high speed $\Delta\Sigma$ ADC

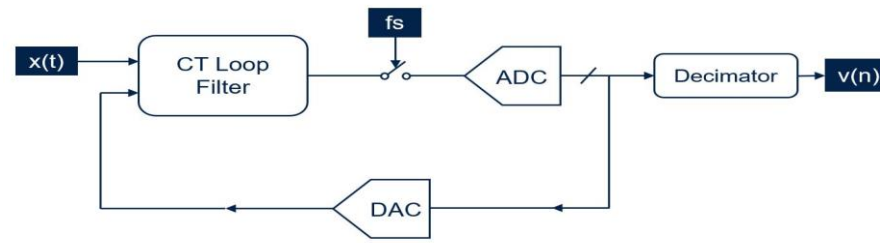
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Motivation

- High speed Analog to Digital Converters (ADCs) are used pervasively in applications such as wireless and wireline communications, and high-definition video processing, which demand high signal bandwidth (20-100MHz) and dynamic range (> 70 dB).
- $\Delta\Sigma$ ADC is a combination of multiple blocks integrated in a loop, traditional small signal simulation techniques cannot be used. Transient simulation needs to be run for the verification of the ADC.
- In this paper, two ADCs combined with Bias block are to be simulated where, each ADC is third order multi-bit and sampled at 3.2 GHz with an input bandwidth of 40 MHz
- Power consumption of this kind of systems can easily go beyond 50 mW leading to challenging power signoff.



Continuous Time $\Delta\Sigma$ ADC

Challenges

For designs with stringent SNR/SFDR specifications, simulation complexities increase many fold

Challenges	Complexity
Multiple blocks integrated together	<ul style="list-style-type: none">• Huge netlist size• Longer simulation times• Tool capacity limitation
High sampling rates	<ul style="list-style-type: none">• Smaller time steps of simulator for accuracy• Multifold increase of parasitic effects
High power consumption	<ul style="list-style-type: none">• Layout routing complexity increases• EM/IR signoff becomes costlier

Power signoff

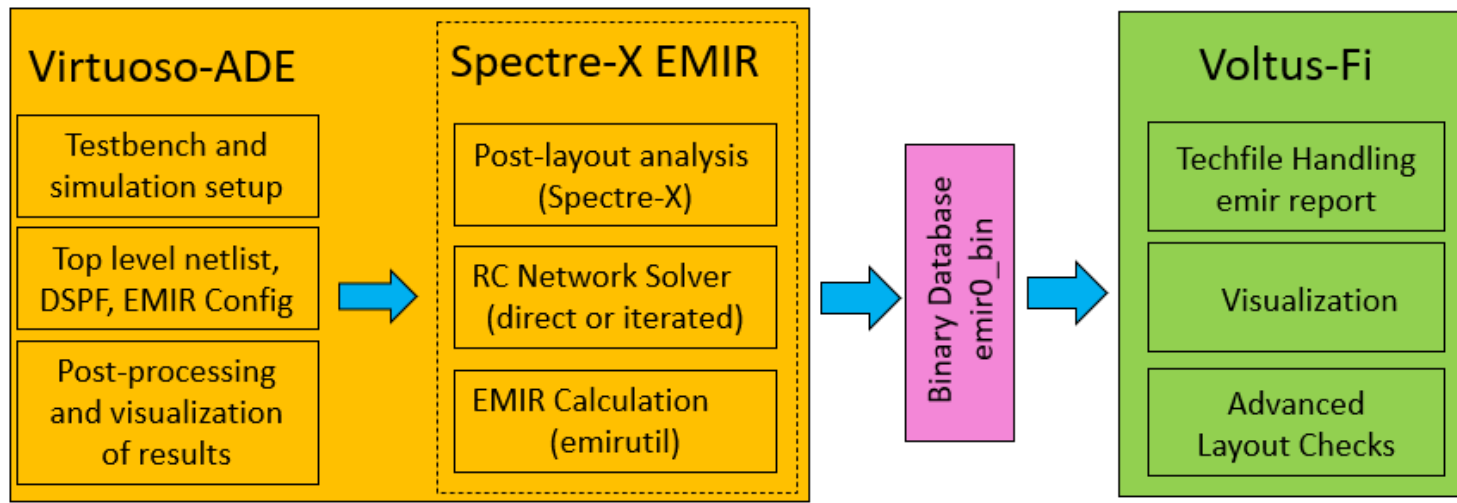
- EMIR flow simulation has a challenge of large netlist and simulation time.
- It is critical to evaluate EM/IR impacts in the layout cycle in a timely manner to reduce the overall design cycle.

Phenomenon	Impacts
EM	<ul style="list-style-type: none">• The minimum width of routing as per EM rules in power-hungry op-amps/delay sensitive blocks lead to increased parasitics, which can degrade performance.
IR	<ul style="list-style-type: none">• Loss in dynamic supply available for high performance analog blocks such as op-amps leading to performance degradation• Change in delay of various timing cells such as internal clock generator and DAC drivers

- ***Design and Layout co-optimization*** becomes critical in high-speed, high-performance ADCs due to the above EM/IR impacts.
- Requires ***multiple and quick iterations***.
- EM/IR signoff becomes costly due to the challenges discussed in the previous slide.

Simulation methodology

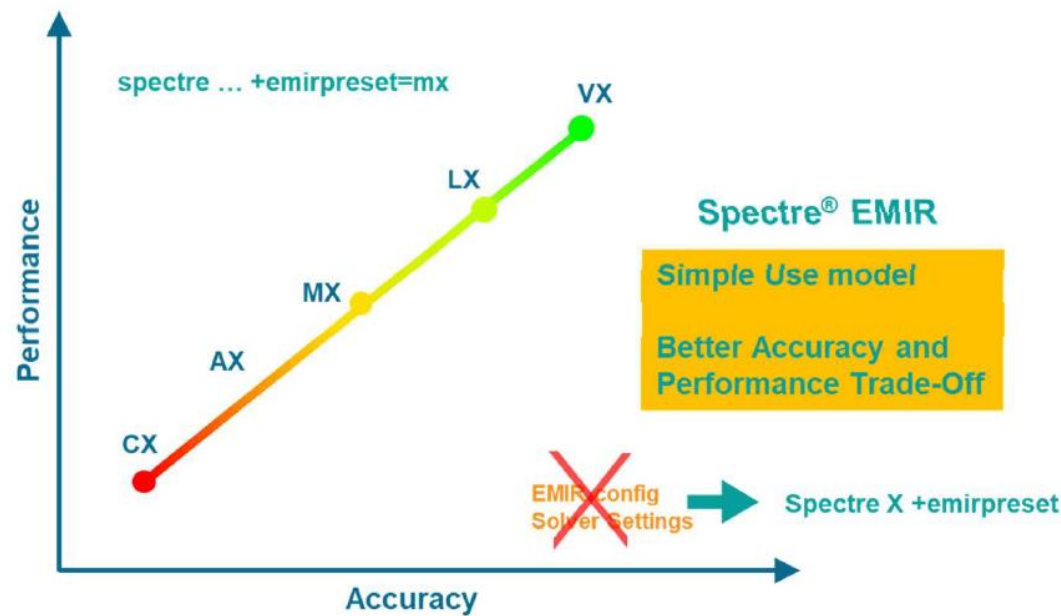
- Setup in Virtuoso ADE-Assembler provides the following advantages to the designers :
 - Common setup environment for multiple analyses eliminating the need of switching design flows.
 - Use of same expressions for pre- and post-layout simulations reducing the setup time.
 - The simple preset use-model and single setting of Spectre-X used across multiple analysis eliminates the multiple iteration cycles to fine-tune the simulator settings.
 - In built Spectre-X EMIR flow integrated with Voltus-Fi for results visualization and post-processing.



EMIR Simulation Flow

EMIR simulation

- The challenge with the existing iterated method is the complex EMIR control file setup required to achieve the best accuracy and performance trade-off.
- Used the Spectre-X solver with a **new simplified emir preset-based use model** for the iterated method that provides a significantly improved performance and gives accuracy close to direct method.
- The new Spectre-X EMIR iterated use model is enabled by setting the **+emirpreset** option that predefines all 1st and 2nd stage EMIR settings.



Simple preset use model for EMIR analysis

Spectre-X EMIR (conventional iterated method)	Spectre-X EMIR (new iterated method)
rcr=selected	+emirpreset=vx
rcr=selected, signal net RCR, power net RCR/REFF	+emirpreset=lx
rcr=asis +postlayout OR new Spectre EMIR users	+emirpreset=mx

EMIR setup

Summary Information

Options	Value
net	name=[ICT1.DGND] analysis=[vmax vavg lmax lavg]
net	name=[ICT1.DVDD] analysis=[vmax vavg lmax lavg]
net	name=[ICT1.AGND] analysis=[vmax vavg lmax lavg]
net	name=[ICT1.AVDD] analysis=[vmax vavg lmax lavg]
net	name=[ICT1.REFM] analysis=[vmax vavg lmax lavg]
net	name=[ICT1.REFP] analysis=[vmax vavg lmax lavg]
include	
emirutil	
emirutil	
emirutil	
solver	method=[iterated]
time	window=[1.2u 1.5u]

pf.emir_conf
/PLS_QRC/6U1x_2T8x_LB/mos028fdsol_6U1x_2T8x_LB_EM_only.ict
x2ict.layermap
xex2oa_qrc.layermap

4. Solver settings and time window in EMIR analysis needs to be enabled

1. nets from the schematic to be analyzed for EMIR

2. emir_conf file from spfchecker

3. Ict and layer map files

OK Cancel Defaults Apply Help

EMIR Analysis Setup

High-Performance Simulation Options

Simulation Performance Mode: Spectre AP **Spectre X** Spectre FX

General

Accuracy + Speed

Preset: CX AX **MX** LX VX

Multi-Threading Multi-Processing

Auto Disable **Manual** # Threads: 1sf

Advanced Options

MS Options

Enable MS

Post-Layout Settings

Instance Preservation: None Selected

Selected Instances:

OK Cancel Defaults Apply Help

Spectre-X setup

Environment Options

Switch View List: admsVerilog veriloga spectre

Stop View List: admsVerilog veriloga spectre

Parameter Range Checking File:

Print Comments

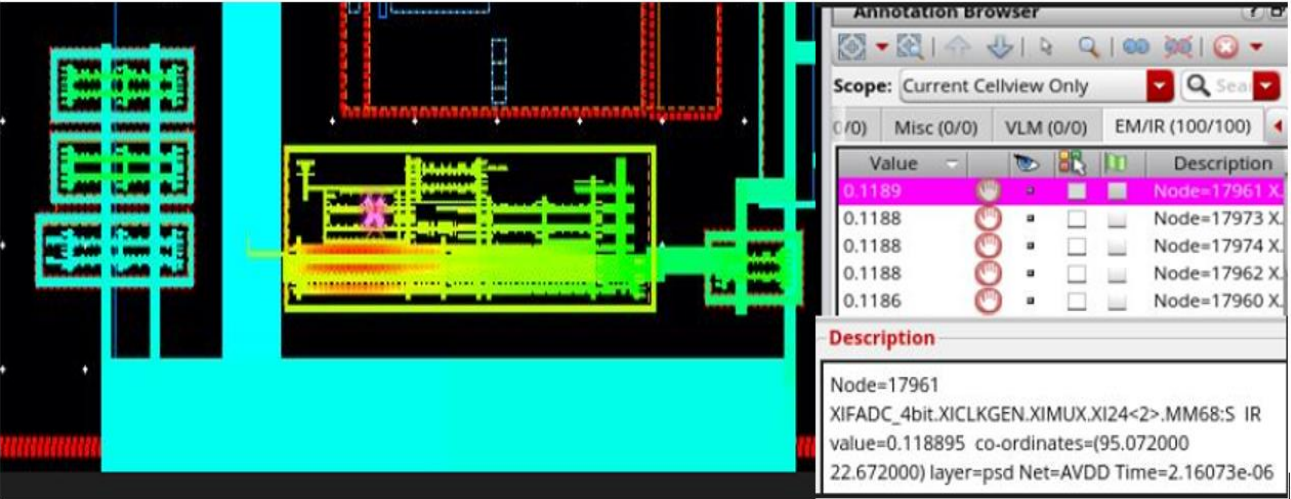
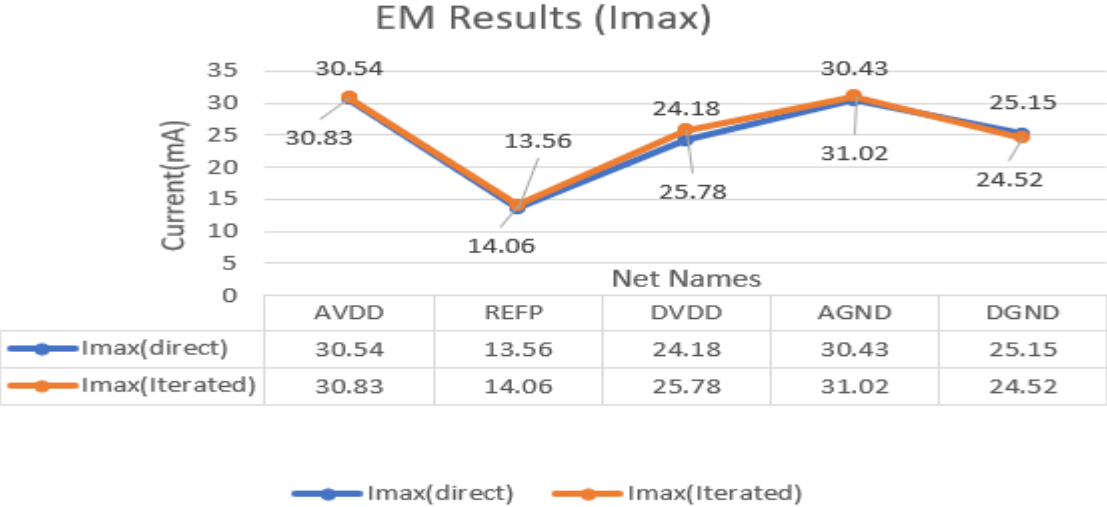
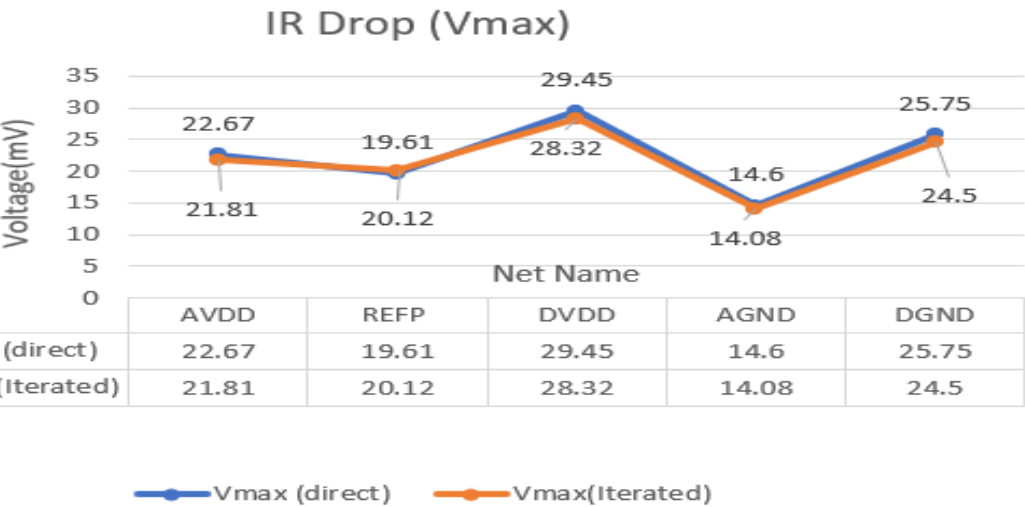
NameMapping SubcircuitPortConnections

User Command-Line Options: **6** +emirpreset=mx

Automatic Output Log

Additional option to enable new iterated method

EMIR results

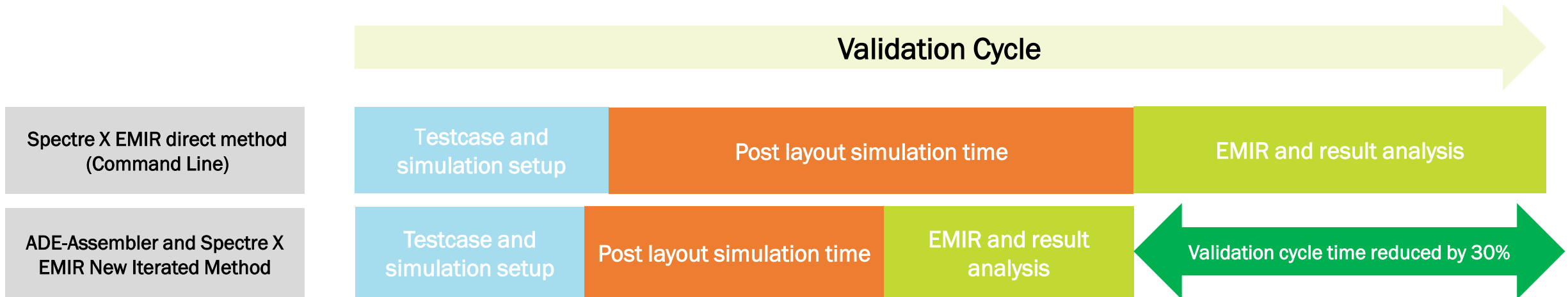


Visualization in Voltus-Fi

Mode	Time Elapsed
+preset=mx Method=[direct] Window[1.2u 1.5u]	4d11h20m
+preset=mx +emirpreset=mx Method=[iterated] Window[1.2u 1.5u]	1d19h30m (2.5X Faster)

Summary

- Successfully able to meet the accuracy target of **SNR=85dB** and **SFDR=83dBc** with Spectre-X for post-layout simulation with **2X performance gain** as compared to existing solution.
- Achieved **1.75X productivity gain** with ADE-Assembler new post-layout simulation features as compared to earlier existing methodologies.
- Successful EMIR signoff closure is done with new Spectre-X EMIR two stage iterated method with exceptional **2.5X performance gain** as compared to direct method. and close to golden accuracy.
- The overall validation cycle is reduced by 30%.





**THE CHIPS
TO SYSTEMS
CONFERENCE**

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Thank you!

